parallel lines extending in a first direction and lying in a first plane;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of vias arranged such that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective one of the plurality of vias, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

5. (Amended) The capacitor of claim 1, further comprising:

at least a third level of electrically conductive